



**1** A FASTER OR SLOWER TIMEOUT CAN BE ACHIEVED BY CHANGING RESISTOR VALUES

**2** 1500 VRMS ISOLATION

**3** Keep signals between chips U12 and T1 as short as possible.

**4** Place inductor L1 as close to U13 as possible.

**5** Group power supply as tightly as possible.

**6** Keep signals as short as possible.

**7** Place R1 - R6 & R29 - R34 on Ground/Back side of board. Place remaining SMT Resistors & Caps. on back at discretion.

**8** Place Components using a logical Data flow as placed in schematic.

**9** 1. Layout Power and Ground first.

**10** MAINTAIN AT LEAST .110" BETWEEN NON-ISOLATED AND ISOLATED SIDES OF THE PCB

**11** {VALUE} TH REPLACEMENT

**12** Model 4850FDR PCBID# 5287R1

**13** Size C

**14** Number FULL/HAUF DUPELEX DC/DC

**15** RS-485/RS-485 OPTICAL ISOLATOR

**16** Date 12/4/01

**17** Drawn by: Doug A.

**18** Sheet 1 of 1

**19** Rev 3

**20** Filename 4850pdr3.SCH